APD’s and Front End Electronics

Getting to a realistic design for the proposal.

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APD's

- ***Where we are now:***
  - Using existing packaged APD's we have shown that the electronics noise level is < 300 electrons.
  - This should get better because:
    - » The APD is not optimized for the detector.
    - » The pre-amp is not optimized for the detector.
- ***What do we still need to know:***
  - Is $2.50/channel a reasonable number?
  - Do we have an advanced enough design to pass a proposal review?
    - » The system requirements of low-temperature, low-light, low-noise and high-volume make this a high risk item that will be scrutinized carefully in any proposal.
  - Several detector other design choices are coupled to the APD configuration.

Restatement of the Problem:

- ***Couple 1,780,000 fiber ends to a sensitive bare silicon device.***
- ***Align each fiber end to make good optical contact with a 1.1 x 2.3 mm^2 pixel.***
- ***Encapsulate each APD in light-tight thermally controlled environment.***
- ***Connect the APD to electronics with a niose floor of 300 electrons or less.***

This is a tough engineering problem which we are sure we know how to solve.
We need some effort now to be convincing that we are right.

Before Proposal

"The purpose of a proposal is to get approved." V. Hughes.

- ***For a detector design to get approved – criticisms that your costs are pie-in-the-sky must be avoided.***
- ***We do not need to detailed engineering – but we do need some engineering.***
  - **Conceptual design of the APD housing, mounting and layout.**
  - **Some thermal modeling to show that cooling is feasible.**
- ***We do need to maintain the current level of interest in our project at Hamamatsu.***
- ***We do not need to make detailed mechanical designs.***
- ***We do not need to make prototype APD modules.***

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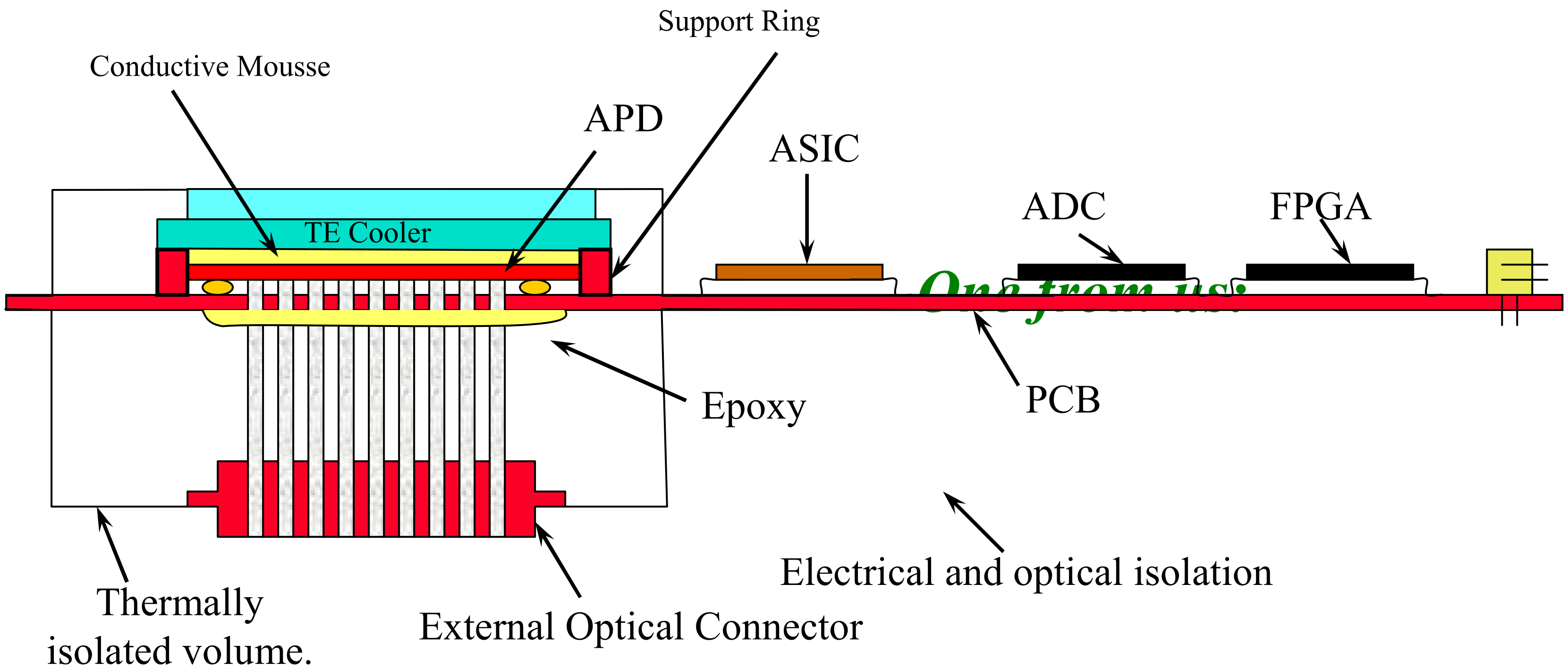
Conceptual Designs

Two suggestions so far:

One from us:



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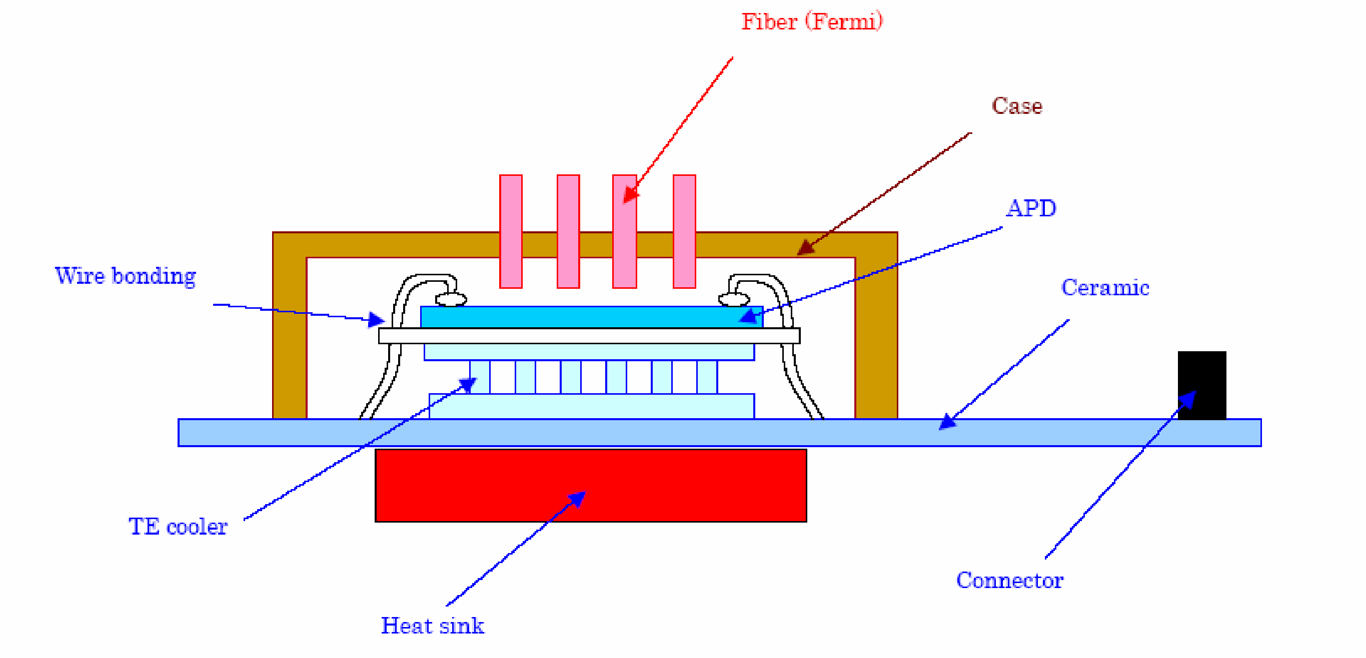
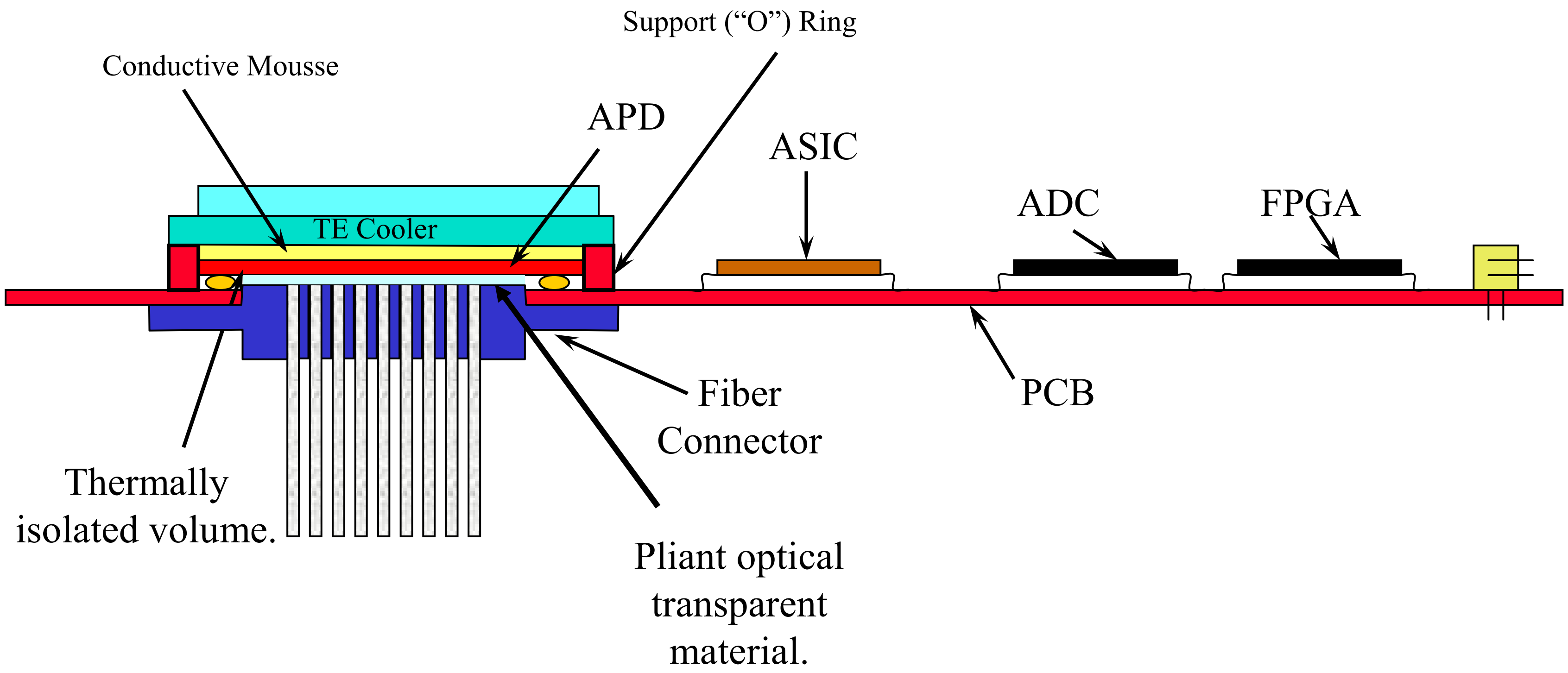
Conceptual Designs

One from Hamamatsu:



Another Possibility



Proposal for this Year's R&D.

- ***Hamamatsu will design with us a the APD module. Solve the following problems:***
  - **High-volume alignment of the fibers to the APD.**
  - **High-volume housing and cooling.**
  - **Advance engineering to point where a defensible cost estimate can be made.**
  - **Confirm operational requirements for bare dies.**
- ***We will not:***
  - **Manufacture new format APD's.**
  - **Manufacture a final version of the APD housing..**

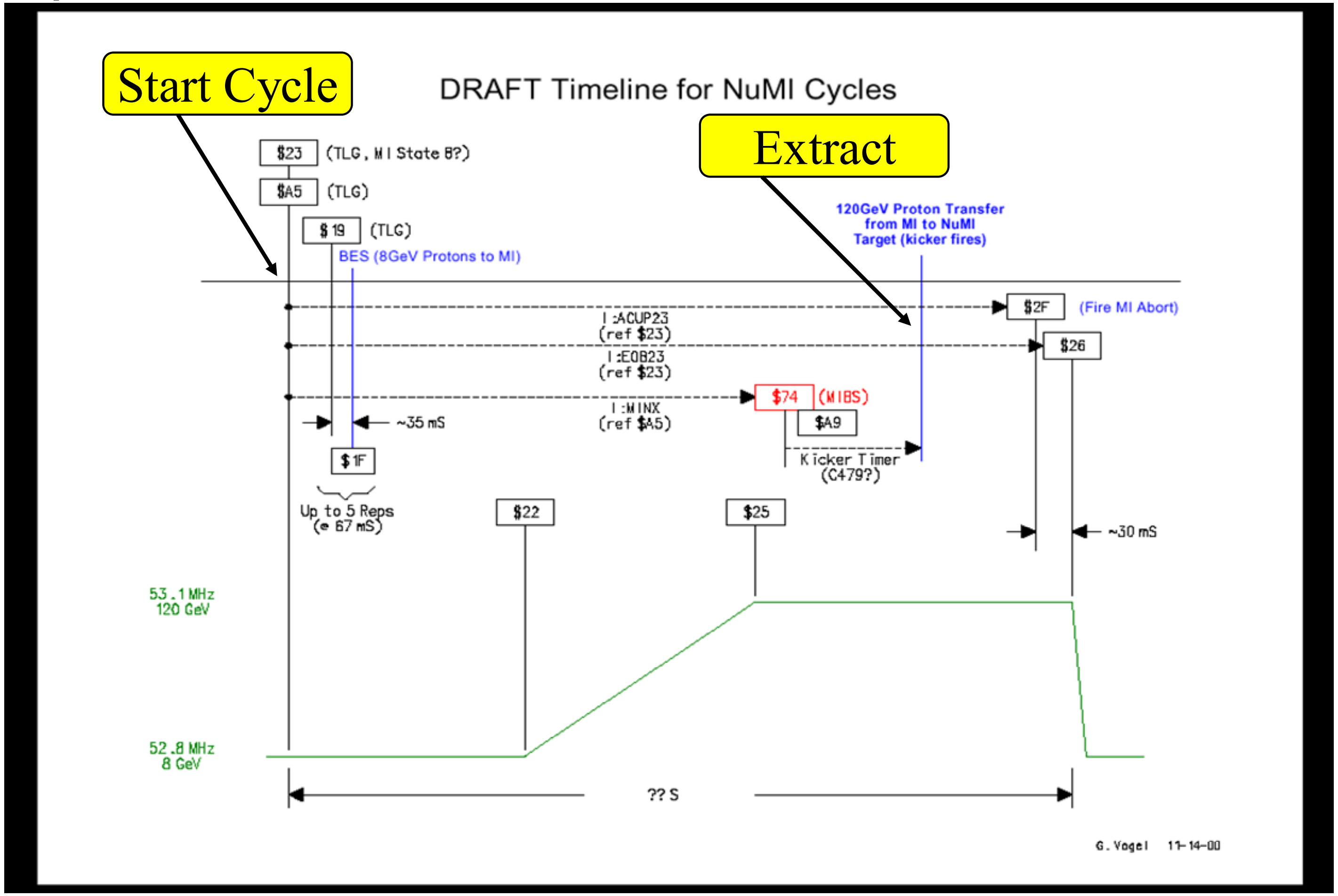
Front-End Readout options.

- ***Several options have been considered for the design of the front-end readout the APD.***
- ***People involved:***
  - **John Oliver (Harvard)**
  - **Tom Zimmerman (FNAL)**
  - **Leon Mualem and Roger Rusack (Minnesota).**
- ***Others who have provided input are:***
  - **Jason Felt, Paul Rubinov, Jon Urheim, Alfons Weber and Ray Yarema.**
- ***Purpose is to consider possible designs and recommend to collaboration development path that ensures we have the best design for Nova.***

Issues

- *MASDA chip is a dual correlated sampling amplifier. It compares signal before and after the event and amplifies the difference.*
  - It is optimized for 70 pF not 10 pF – higher noise.
  - Is not pipelined – not suitable for final design.
- *Optimize for Nova:*
  - Readout whole spill.
  - Provide time slices with higher resolution than 500 nsec.
  - More advanced digital filtering. (Use more pre and post data to surpress noise.)
- *Precision of prediction of the arrival at the far detector. – Alfons Weber.*
- *What about supernova's?*

MI Timing Events (I)



MI Timing Events (II)

- Signals available
  - Start of NuMI cycle (earliest)
    - ~1.4 sec in advance: $23 & $A5 (yet unknown, but fixed)
    - predicts spill to within +/- 5.5 μsec
  - Kicker fire (most accurate)
    - few 1 μsec – 1 msec in advance: $74
    - spill-to-spill jitter: few nsec
- Not possible to predict from one spill when the next will happen
  - Timeline can change on a 1 min basis

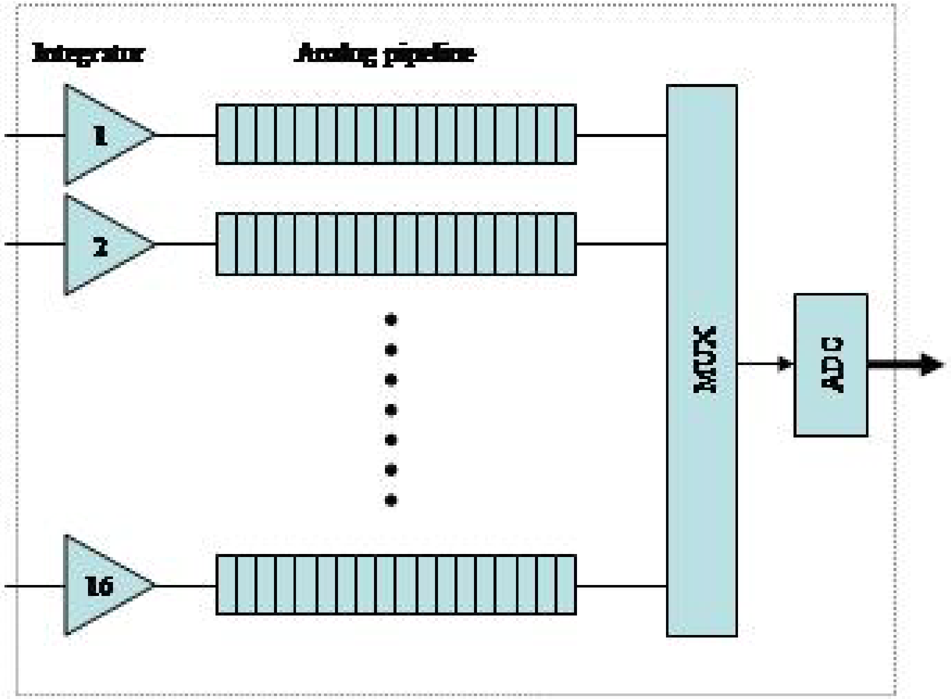
Timing Conclusion – Alfons Weber.

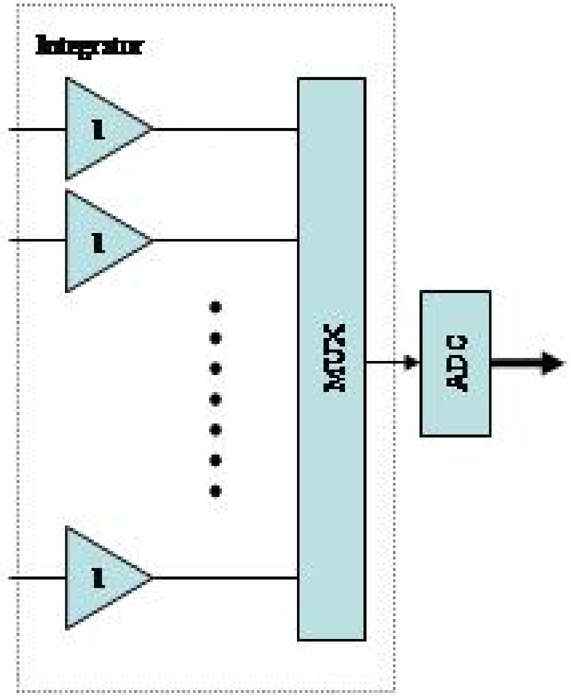
Conclusion

- Spill trigger & signal transmission have to be included in design from the beginning
- No latency needed in FE
- But, needs >20 μsec lifetime of FE

So a readout requiring a spill signal is feasible.

ASIC Options Considered.





Option 1.
Accumulate signal during spill & digitize after spill.

Option 3.
Continuous accumulate and digitization of signal during.

Pros and Cons

- ***Option 1.***
  - Low-risk design, leverage from SVX-4 and MASDA.
  - Signal acquisition and conversion occur at at different times.
  - Requires spill signal.
- ***Option 3.***
  - ~100% Live-time.
  - Smaller die size.
  - Simultaneous signal acquisition and digitization – requires careful design to keep noise level low.

Recommendations:

1) The design of option 1 should be started immediately. This design is optimized for the theta-13 measurement but is not suitable for supernova detection. The benefits of low risk match the need to quickly demonstrate that the whole detector concept is feasible. This should remain our baseline design until the viability of the supernova detection with the detector has been established and a realistic performance test has demonstrated option 3.

2) The design study of option 3 should be continued. The higher risk of this readout approach should not jeopardize process of proving the detector technology. However, the design can proceed along with the physics studies to understand of the supernova signal. The decision process here is 1) demonstration of proof-of-principle with the discrete prototype currently being tested at Harvard. 2) The design, layout and simulation of an ASIC should be started, which will be followed by an MPW run and a realistic performance test. If at any time during this process it is clear that the supernova signal is unlikely to work, then this effort should be put on hold. The timescale for this decision is later than the need for a working version of option 1 to demonstrate the viability of the detector. The engineering effort for this should, however, be on the project baseline.

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Current Status:

- ***Fermilab:***
  - Tom Zimmerman is currently designing a 64-channel ASIC along the lines of option 1.
  - Status:
    - » Low-noise front-end preamp designed.
    - » Designing the SCA network.
  - To be done:
    - » Incorporate Gray code and ramp generator and comparitor and latch network – most from SV4.
    - » Simulations.
    - » Layout
    - » Post-layout simulations.
- ***Outcome:***
  - Expect to have a design ready for a MPW run mid-2005.

Current Status:

- ***Harvard:***
  - **Discrete component system built to explore feasibility of simultaneous conversion and digitization.**
  - **Tests underway.**
  - **Results will be known soon.**